A Dual-Varactor Analog Phase Shifter Operating at 6 to 18 GHz

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***Abstract*—An MMIC analog reflection phase shifter achieves 120° of phase shift from 6 to 18 GHz using a dual-varactor reflection circuit which allows varactors with a 3 : 1 capacitance ratio to achieve the performance that normally requires 10 : 1 diodes. The varactor diode is a surface-oriented structure with a hyperabrupt doping profile selectively ion implanted to a depth of 0.70 μm.**

I. INTRODUCTION

A DUAL-VARACTOR reflection phase shifter has been fabricated and tested. The use of a dual-varactor reflection circuit on each of the direct and coupled ports of a quadrature coupler gave an equal-ripple phase shift versus frequency response over 6 to 18 GHz that would otherwise not be obtained by a single-varactor circuit. Typical single-varactor circuits are based on a diode structure comprising a thick n layer on top of an n^+ layer. The thick n layer allows a high capacitance ratio, and the buried n^+ layer lowers series resistance. Monolithic processing of this structure is complicated because the n and n^+ layers must be mesa etched, leaving a high mesa. Also, an air bridge over the mesa edge must be used and has only a small anode dot or finger to which it can make contact. The circuit design of this paper is based on a surface-oriented, selectively ion implanted, hyperabrupt (within the limitations of a Gaussian) varactor with a deep implant rather than a buried n^+ layer. The varactors made by this process had a 3 : 1 capacitance ratio, compared to commercially available diodes with VPE grown layers on n^+ substrates that have greater than 10 : 1 capacitance ratios. The dual-varactor circuit allows 3 : 1 diodes to get the performance of 10 : 1 diodes and maintain a monolithic process.

Measured phase shift was typically 0 to 150° ± 20° with 2.7 dB typical insertion loss (4.0 dB worst case) for one coupler section over 6 to 18 GHz.

II. CIRCUIT DESCRIPTION

The circuit of Fig. 1 shows the dual-varactor reflection circuit. The circuit is patterned after a dual-varactor circuit proposed in [1] for the UHF band and adapted here for the 6 to 18 GHz band. Reverse bias is applied simultaneously to both varactors on each port of the coupler. The circuit resonant at f_1 (zero-bias resonance at 5.4 GHz) results in a phase shift over 6–9 GHz; however, the f_1 circuit is inductive and insensitive to varactor tuning from 9 to 18 GHz. The circuit resonant at f_2 (zero-bias resonance at 25 GHz) is capacitive from 9 to 18 GHz and over 9–18 GHz tunes the inductive f_1 circuit so that phase shift occurs over the 9–18 GHz part of the band. Adding two additional elements (shown in Fig. 2) during optimization gave the best phase flatness. The final circuit element values are given in Fig. 2. The inductors when replaced with the equivalent length of 100 Ω microstrip give the modeled response described below. The coupler of Fig. 2 is slightly overcoupled (K = 2.25 dB) to minimize the

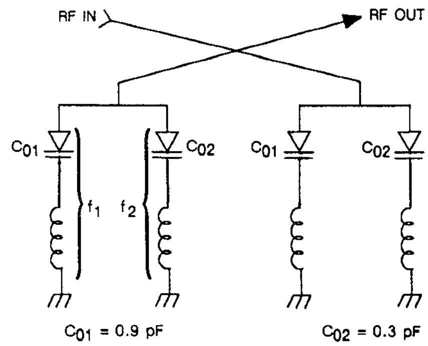

Fig. 1. The combination of the f_1 circuit and the f_2 circuit gives flat phase shift response from 6 to 18 GHz. The varactor-inductor zero-bias resonances, f_1 and f_2, are 5.4 GHz and 25 GHz, respectively.

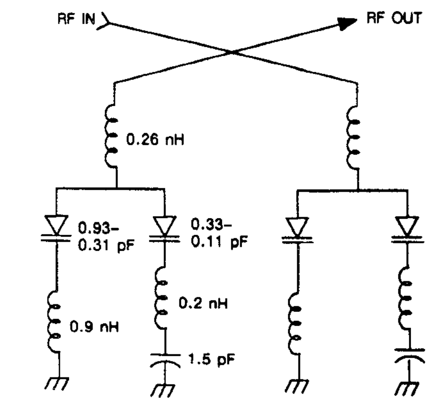

Fig. 2. Elements were added to the circuit of Fig. 1 to help flatten phase shift.

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VSWR by spreading the *VSWR* ripple equally over the 3 : 1 band [2]. The corresponding even- and odd-mode impedances are 142 and 18 Ω, respectively, and the modeled *VSWR* is a maximum of 1.5 : 1 over the 6 to 18 GHz band.

III. Performance Results

Modeled and measured phase shifts are shown in Fig. 3. An equal-ripple response is observed in both the modeled and measured curves. The phase flatness of the measured device is ±20°, and the minimum amount of phase shift is 130° at all points across the band. The corresponding measured insertion loss (Fig. 4) is 2.7 ± 1.3 dB over the frequency and bias control voltage range. Both the modeled and measured curves show the same trend of the zero-bias curve, which has more insertion loss below 12 GHz and less insertion loss above 15 GHz relative to the 8 V curve. The modeled insertion loss curves are different in absolute value by 0.5 dB than the measured curves because a 100 GHz f_{c0} ($f_{c0} = 1/\{2\pi\ R_s\ C_0\}$, R_s and C_0 measured at zero bias) was assumed in the modeled calculations and the varactor as fabricated had 75 GHz f_{c0}. Input/output *VSWR* was measured to have a maximum over frequency and bias control voltage of 2.0 : 1 (Fig. 5) compared to the expected *VSWR* of 1.5 : 1. The coupler as fabricated had 2.0 dB rather than the modeled value of 2.25 dB for the coupling coefficient, which caused greater *VSWR* at band center than necessary. The modeled curves agreed with the measured curves when the coupling coefficient was increased to 2.0 dB. The coupling coefficient of 2.0 dB was measured on a coupler with the diode reflection circuits removed. The measured Z_{0e} was 162 Ω and the Z_{0o} was 18.5 Ω compared to the design values of 142 and 18 Ω. The increase in coupling coefficient ($K = (Z_{0e} - Z_{0o})/(Z_{0e} + Z_{0o})$) was due to an increase in Z_{0e} rather than a decrease in Z_{0o}, and when the increased Z_{0e} is substituted for the $Z_{0e} = 142\ \Omega$ used in the modeled curves, the measured and calculated *VSWR* agree (Fig. 5). The actual physical dimensions of this coupler were: line widths of 15 μm, gaps between lines of 14 μm, and overall coupler length of 0.090 in.

Two-tone, third-order intermodulation products were measured for the different bias states. The zero-bias state had the lowest intercept point, 9 dBm. As the reverse bias was increased from zero to 8 V the intercept point monotonically increased from 9 dBm to 14 dBm. The intercept point could be increased by approximately 9 dB for all bias states by using back-to-back varactors in place of each of the varactors in Fig. 2. The use of back-to-back varactors [4] increases the intercept point by 6 dB due to each single diode being replaced by the series combination of two diodes, each having twice the junction area of the single diode, and an additional 3 dB by the first-order slope in capacitance versus voltage of one varactor canceling the first-order C–V slope of the second (reverse-connected) varactor.

IV. Varactor Modeling and Circuit Optimization

A process for the varactor had already been established, and the varactor capacitance and series resistance varia-

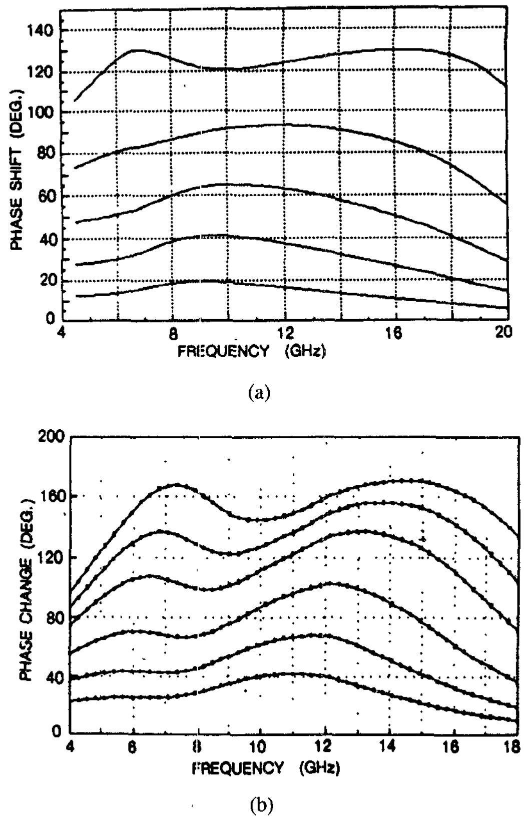

Fig. 3. The (a) modeled and (b) measured phase shift both show the same trends. The measured ripple is greater due to differences in the characteristics of the varactor as modeled versus the measured.

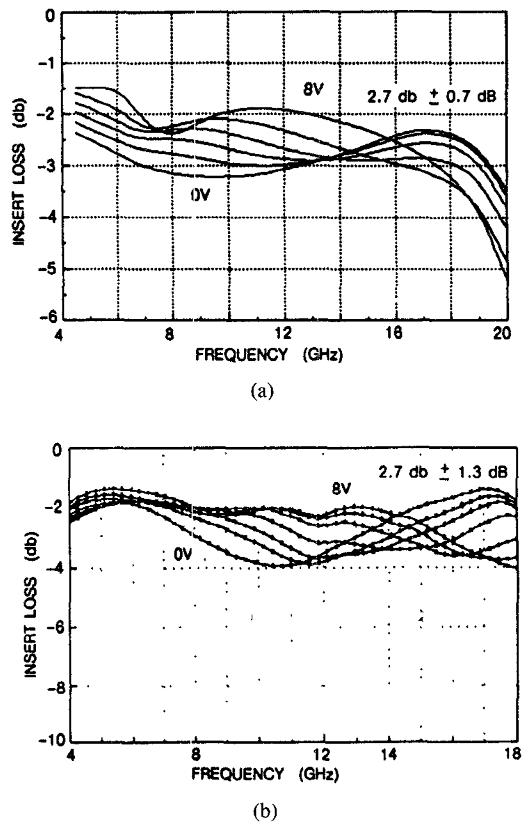

Fig. 4. The (a) modeled and (b) measured insertion loss show the same trends. The measured loss is 0.5 dB higher because measured f_{c0} was 75 GHz versus a modeled value of 100 GHz.

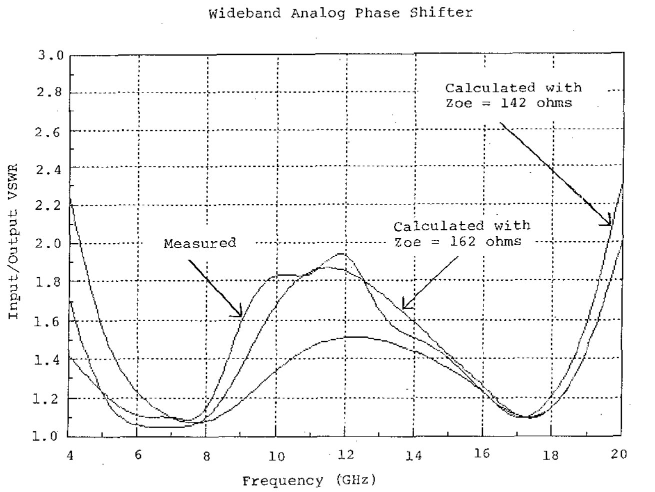

Fig. 5. The calculated and measured curves agree when Z_{0e} is replaced by the measured value of 162 Ω. The worst-case *VSWR* occurred at zero bias, which is the state shown for both the modeled and the measured curves.

tions with bias were known. The f_c as a function of bias was therefore known. During circuit optimization C_{01} and C_{02}, or the area of each varactor, were varied to optimize circuit performance. The R_s parasitic for each varactor was computed from f_c and the area (C_0) for a given bias by computing f_c as a dependent variable with bias as the independent variable. In other words, C_0 was the variable of optimization and $f_c(V)$, $C(V)$, and R_s were computed as dependent variables as C_0 was changed during optimization. The modeled curves of Figs. 3 and 4 include these interdependencies and optimization for minimum insertion loss and insertion loss modulation was done simultaneously as phase shift and phase shift flatness were optimized.

V. Fabrication

The varactor is an anode finger along each side of which there is ohmic metal area. The anode finger is 0.75 μm × 140 μm and the ohmic area on each side of the anode is 10 μm × 140 μm. The ohmic–anode spacing is 1.0 μm. The doping profile under the anode is hyperabrupt and is obtained by selective ion implantation (Fig. 6). The depth of the doping profile is 0.70 μm in order to ensure a conducting layer underneath the depletion region over the range of control voltage. A single $^{28}Si^{++}$ and three $^{29}Si^{+}$ implants were chosen to produce a profile which is doped at 2×10^{17} cm^{-3} near the surface, dropping off to a deep, low-doped tail. The f_{c0} of the varactor was measured to be 75 GHz, and the capacitance ratio was 3:1. Without fringing, the capacitance ratio would be approximately 6:1.

The chip of Fig. 7 is 0.148 in × 0.068 in × 0.015 in. The substrate thickness was chosen to be 0.015 in rather than 0.004 in to make the interdigitated Lange coupler lower loss. A resist thickness and profile appropriate to lift off 4 μm of metal were chosen so that a thicker than usual overlay metal could be used to lower the loss of the coupler while maintaining better dimensional control than that offered by a plating process. The coupler loss was

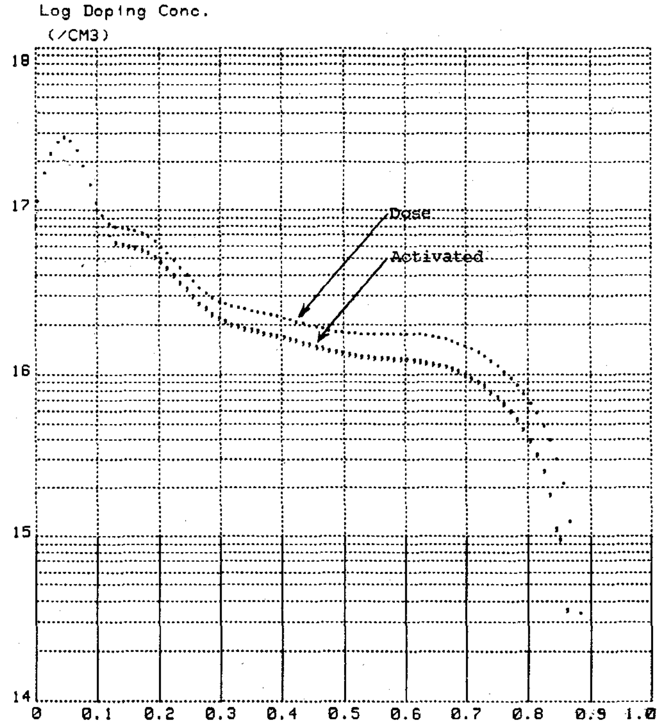

Fig. 6. The doping profile was obtained by ion implantation at a depth of up to 0.70 μm.

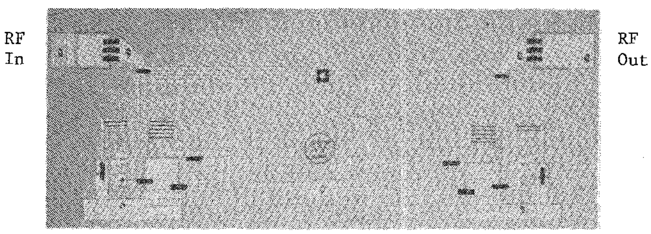

Fig. 7. The phase shifter chip size is 0.148 in × 0.068 in × 0.015 in.

measured to be 0.25 dB (for single pass) above the coupling losses.

VI. Comparison with Present and Prior Art

It is interesting to note how different approaches to improving varactors for MMIC applications have evolved over the last seven years. Surface-oriented varactors with capacitance ratios greater than 10:1 were reported in [3], but as pointed out there the high capacitance ratio was obtained under the condition of punch-through, with the result that the varactor Q degraded just before punch-through. Based on avoiding varactor punch-through, a flat-profile, ion-implanted thick layer was reported in [4]; a flat profile ramping up to an ion-implanted thick n$^+$ layer was reported in [5]; an MBE hyperabrupt profile on n$^+$ (mesa structure) was reported in [6]; and in this work a hyperabrupt ion-implanted thick layer (Fig. 6) is reported.

With respect to the circuit design, single-varactor reflection circuits implemented monolithically were reported at *X*-band in [4] and at *Ku*-band in [6]. Each of these two designs was of less than 40 percent bandwidth. In the hybrid circuit area, 150+° of phase shift from 6 to 18 GHz was reported in [7] using a single-varactor design with 15:1 discrete chip varactors. Also, binary phase modulators using two p-i-n diodes in a dual-diode reflection circuit configuration were reported in [1] with measured results over several octaves in the UHF band. A dual-varactor analog circuit was proposed in [1] where computer simulation of the circuit was done at UHF over octave-plus bandwidths, but measured results were not presented.

The diode design discussed above and the dual-diode reflection circuit discussed above have been combined to achieve broader band monolithic analog phase shifter performance than reported to date.

VII. Conclusion

An analog, 6 to 18 GHz, 120° phase shifter has been fabricated and measured. A dual-varactor reflection circuit obtained 3:1 bandwidth using varactors with a 3:1 capacitance ratio, a result that has not been achieved by single-varactor circuits. Discrete chip varactors with a 15:1 capacitance ratio and 0–30 V bias control voltage were used in a single-varactor hybrid circuit with 150-plus degrees of phase shift over 6 to 18 GHz [7], but the dual-varactor circuit allows a low-cost, ion-implanted, monolithically compatible process to achieve performance suitable for wide-band applications.

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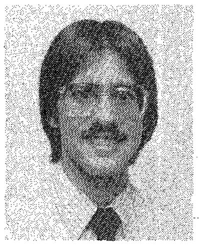

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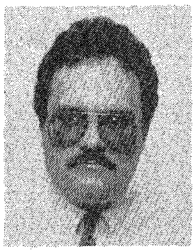

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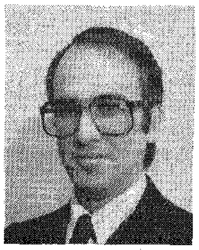

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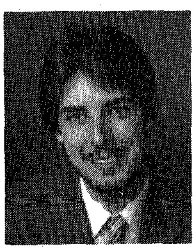

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